Complete FPGA-based SmartNIC solution

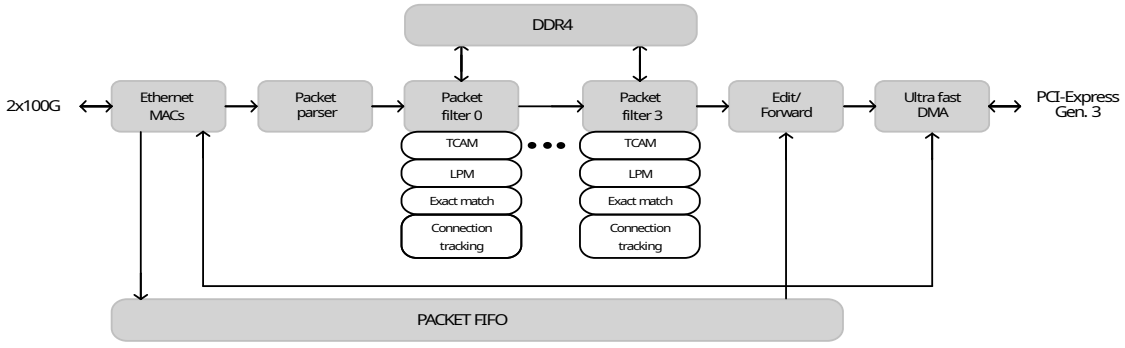
on Alveo U200 hardware from

AMD XILINX

SmartNIC (Smart Network Interface Card – NIC) is a specialized network adapter that **offloads certain processing tasks** from the host CPU to the NIC itself. These tasks can include **packet filtering, encryption/decryption, compression**, and other functions that are typically performed by software running on the host. By moving these tasks to the SmartNIC, it reduces the load on the host CPU, **increases network performance and significantly improves overall efficiency.** The **FPGA allows for flexibility** in terms of the specific tasks that can be performed, as well as the **ability to easily update or modify the SmartNIC's functionality** as needed.

How DYNANIC makes complete solution on Alveo U200?

Programming FPGA is not an easy task. DYNANIC **comes with the universal high-speed FPGA packet processing pipeline** for Alveo U200. This pipeline consists of components required for various packet processing in many use-cases. And so DYNANIC **enables full utilization of FPGA-technology without prior FPGA knowledge!**



This wire-speed capable FPGA pipeline is **controlled from the host software** by standardized and open-source RTE Flow DPDK API. For example, to set up the filtration rule in the pipeline, it is only needed to write **a few lines of code in C++ or Python** programming language. So simple!

Use-cases with DYNANIC

Network acceleration

Examples of processing tasks that can be offloaded with DYNANIC include packet processing, encryption/decryption, compression/decompression or implementation and acceleration of future network protocols.

Network security

Example applications are firewall, intrusion detection and prevention systems (IDS/IPS), and DDoS mitigation (Anti-DDoS). All these can be offloaded with DYNANIC for improving performance and reducing latency.

Network monitoring and analyses

Troubleshooting network issues, detecting anomalies, and identifying performance bottlenecks with full wire-speed traffic capture in real time is possible thanks to DYNANIC.

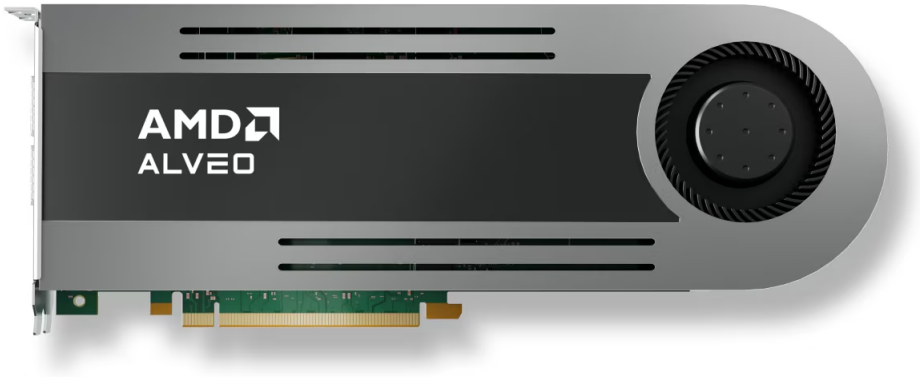
Content delivery

DYNANIC can help applications for accelerating content caching and delivery, improving user experience and reducing server load in content delivery networks (CDNs).

Virtualized networking

Virtualized networking functions (NFV) such as virtual switches and routers improve performance and reduce latency using DYNANIC solution.

And many more . . .



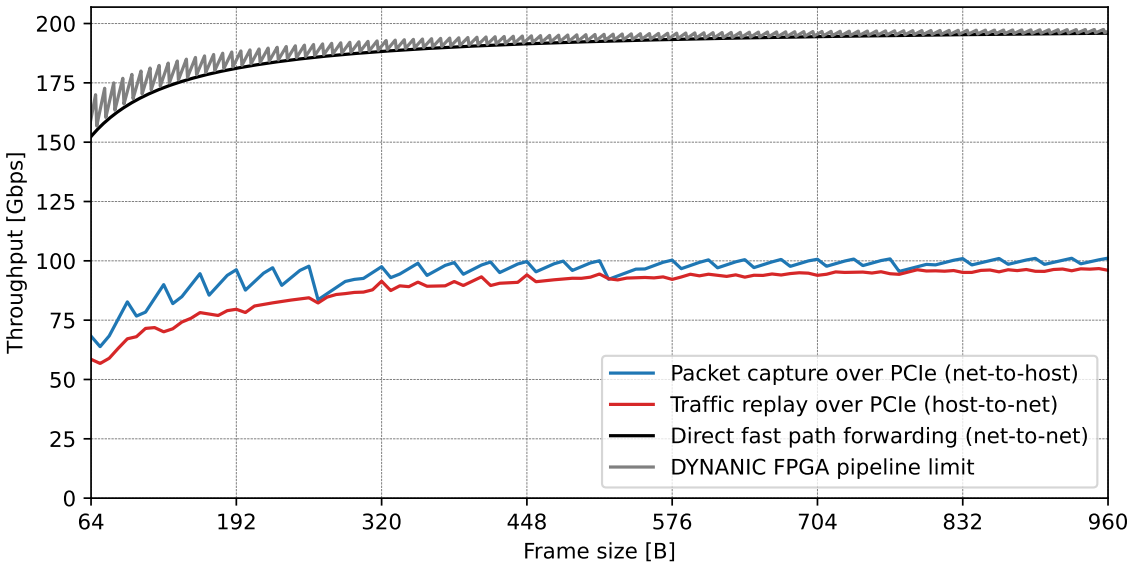
Alveo U200** by **AMD/Xilinx.

Unique features of DYNANIC solution on Alveo U200

- **No need for FPGA** development, processing pipeline is given
- **Standardized and open-source** DPDK software stack
- **Processing pipeline controlled** by standard RTE Flow interface
- **Full 100 Gbps throughput** to and from host RAM
- **Configurable packet** parser supporting protocols from L2 to L4
- **Different filtering options utilizing** internal or external memories
- **Flow tracking** with fast atomic insert/removal from host
- **Solution ready** for different link speeds even on given card
- **Lossless traffic** processing at wire-speeds from 10G to 100G.

Link speed configuration	Exact match	LPM prefixes	TCAM rules
10/40 Gbps	2.3 M	1.3 M	20 k
100 Gbps	2.3 M	1.3 M	10 k

*Achievable rule capacity for different filter types on **Alveo U200**. Values provided for IPv4 address matching. Exact match and LPM can be combined by sharing the capacity.*



*DYNANIC throughput measurements on **Alveo U200** with 2x100GbE and PCIe gen3. On-chip pipeline is calibrated for sustained wire-speed processing with a small margin on top. The only performance bottlenecks are introduced by the overhead of DPDK transfers over PCIe.*

DYNANIC

DynaNIC Semiconductors Ltd. offers custom design and development services for FPGA-based projects. For more than 20 years are company team members specializing in the acceleration of algorithms required for high-speed network packet processing (e.g. packet parsing, packet/headers fields extraction, hash based pattern matching, filtering, traffic flow management, etc.) with link speeds up to 400 Gbps. Unique portfolio of IPs was also utilized to bring FPGA technology closer to any software company. That's how the flagship **DYNANIC** solution was created.

AMD

XILINX

AMD is the high performance and adaptive computing leader, powering the products and services that help solve the world's most important challenges. Their technologies advance the future of the data center, embedded, gaming and PC markets since 1969. The acquisition of Xilinx brings together a highly complementary set of products, customers and markets combined with differentiated IP and world-class talent. Adding industry-leading FPGAs, adaptive SoCs, AI inference engines and software expertise enables AMD to offer the strongest portfolio of high-performance and adaptive computing solutions in the industry and capture a larger share of the market across cloud, edge, and intelligent devices.

How to start?

Contact AMD/Xilinx to obtain Alveo U200 at their website

and visit

DynaNIC website to download working package for Alveo U200.